IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Atila Alvandpour *et al.*	Examiner:	Anh Q. Tran
Serial No.:	10/010,737	Group Art Unit:	2819
Filed:	December 7, 2001	Docket:	884.451US1
Assignee:	Intel Corporation	Customer No.:	21186
Title:	VOLTAGE-LEVEL CONVERTER		

APPELLANTS' BRIEF ON APPEAL

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on November 11, 2003, from the final rejection of claims 1-25 of the above identified application, as set forth in the final Office action mailed on June 11, 2003.

This Appeal Brief is filed in triplicate and accompanied by authorization to deduct the requisite fee set forth in 37 C.F.R. § 1.17(c).

Real Party in Interest

The real party in interest of the above identified application is the Intel Corporation as identified in the assignment recorded on March 12, 2002 (Reel/Frame 012701/0934) (3 pages).

Related Appeals and Interferences

There are no appeals or interferences known to appellants, the appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the decision of the Board of Patent Appeals and Interferences in the pending appeal.

Status of Claims

Claims 1-25 are currently pending and appealed.

Status of Amendments

No amendments were proposed after the final Office action (mailed on April 11, 2003).

Summary of Invention

A logic unit includes a first logic unit, a second logic unit, and a voltage level converter. The first logic unit is connected to a first supply voltage. The second logic unit is connected to a second supply voltage. The voltage-level converter connects the first logic unit to the second logic unit. The voltage-level converter includes at least one transistor having a threshold voltage greater than or about equal to the difference between the second supply voltage and the first supply voltage and the at least one transistor connected to the second supply voltage.

Issues

Whether the patent office erred in rejecting claims 1-7, 9-11, and 23-25 as being unpatentable over Aoki (U.S. Patent No. 5,610,544) in view of Nunogami (U.S. Patent No. 5,136,191) under 35 U.S.C. § 103(a).

Whether the patent office erred in rejecting claims 8 and 17 as being unpatentable over Aoki (U.S. Patent No. 5,610,544) in view of Nunogami (U.S. Patent No. 5,136,191) and further in view of Tanaka *et al.* (U.S. Patent No. 6,249,145) under 35 U.S.C. 103(a).

Whether the patent office erred in rejecting claims 12-22 over Aoki (U.S. Patent No. 5,610,544) in view of Nunogami (U.S. Patent No. 5,136,191), Tanaka *et al.* (U.S.

Patent No. 6,249,145), Aizaki (U.S. Patent No. 5,115,434) and in further view of LaRue *et al.* (U.S. Patent No. 5,027,007) under 35 U.S.C. § 103(a).

Grouping of Claims

Claims 1-7, 9-11, and 23-25 stand together for purposes of this appeal. Claims 8 and 17 stand together for purposes of this appeal. Claims 12-22 stand together for purposes of this appeal.

Argument

Rejections Under 35 U.S.C. 103(a)

Each of the claims 1-25 was rejected under 35 U.S.C. §103 using a combination of references. Claims 1-7, 9-11, and 23-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Aoki (U.S. Patent No. 5,610,544) in view of Nunogami (U.S. Patent No. 5,136,191). Claims 8 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Aoki (U.S. Patent No. 5,610,544) in view of Nunogami (U.S. Patent No. 5,136,191) and further in view of Tanaka et al. (U.S. Patent No. 6,249,145). Claims 12-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Aoki (U.S. Patent No. 5,610,544) in view of Nunogami (U.S. Patent No. 5,136,191), Tanaka et al. (U.S. Patent No. 6,249,145), Aizaki (U.S. Patent No. 5,115,434) and in further view of LaRue et al. (U.S. Patent No. 5,027,007).

Claims 1-25

The Office action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re* Sang Su Lee, 277 F.3d 1338 (Fed. Cir. 2002). The Office action fails to meet this burden. The statements in the Office action as to why the combinations would be obvious do not constitute specific, objective evidence of record. They are merely conclusory statements.

For example, as to the combination of Aoki and Nunogami, which is required for all of the rejections, the Office action, at the bottom of page 2 and the top of page 3, states:

> Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the at least one transistor (61, Fig. 3) of Aoki having a threshold voltage greater than or about equal to the difference between the second supply voltage and the first supply voltage as taught by Nunogami in order to transfer a signal without troubles.

However, nothing in this statement explains the reasoning that connects the specific, objective evidence of record to the finding of a suggestion or motivation to combine the reference teachings. Note that Fig. 3 of Nunogami (specific evidence of record) includes the transistor of interest (PMOSFET 11 of Fig. 1 of Nunogami) embedded in a complex feedback circuit (feedback loop includes path from junction 18 to node 38, through CMOS circuit 33, through PMOSFET 32, to junction 37, through capacitor 31 to NMOSFET 28), while Fig. 3 of Aoki (specific evidence of record) shows a two-transistor inverter. The Office action does not explain how the transistor of interest embedded in the complex feedback circuit of Nunogami suggests an application to a two-transistor inverter circuit of Aoki. Applicant respectfully submits that the complex feedback circuit of Nunogami does not suggest an application to a two-transistor inverter circuit of Aoki. Hence, the Office action fails to meet the standard established by *In re* Sang Su Lee for finding a suggestion or motivation to combine the reference teachings.

Thus, the final Office action failed to state a *prima facie* case of obviousness with respect to claims 1-25. Therefore, the patent Office erred in rejecting claims 1-25 as being unpatentable over Aoki in view of Nunogami under 35 U.S.C. § 103(a).

Claims 8 and 17

As to the combination of Aoki and Nunogami with Tanaka *et al.* which is required for the rejections of claims 8 and 17, the Office action, at the bottom of page 2 states:

> Akoi in view of Nunogami discloses the claimed invention except for the second logic unit comprises a clock distribution circuit. Tanaka discloses a second logic unit (602, Fig. 14) comprises a clock distribution circuit. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the logic unit (3a) of Aoki having a clock distribution circuit, in order to provide clock distribution signals.

In essence, this statement says that the reason that Akoi and Nunogami can be combined with Tanaka *et al.* is that adding a clock distribution circuit to the logic unit (3a) of Aoki provides clock distribution signals. That reasoning is circular and fails to meet the standard of *In re* Sang Su Lee. The statement fails to cite to specific, objective evidence of record that supports the finding of a teaching, suggestion, or motivation to combine Akoi and Nunogami with Tanaka *et al.*

Furthermore, Fig. 3 of Akoi shows a buffer circuit, Fig. 3 of Nunogami shows an interface circuit, and Fig. 14 of Tanaka *et al.* shows a level conversion system. The Office action fails to show how these references may be combined to produce a functional circuit, so the Office action not only fails to meet the standard of *In re* Sang Su Lee, the Office action fails at a more fundamental level. Without a showing of a functional circuit, it is clear that there is no teaching, suggestion, or motivation to combine the references.

Thus, the final Office action failed to state a *prima facie* case of obviousness with respect to claims 8 and 17. Therefore, the patent office erred in rejecting claims 8 and 17 as being unpatentable over Aoki in view of Nunogami and further in view of Tanaka *et al.* under 35 U.S.C. 103(a).

Claims 12-22

As to the combination of Aoki and Nunogami and Tanaka *et al.* with Aizaki and LaRue *et* al. which is required for the rejections of claims 8 and 17, the Office action fails to provide any reasoning for applying Aizaki to the rejection, so the Office action fails to meet the standard of *In re* Sang Su Lee.

Thus, the final Office action failed to state a *prima facie* case of obviousness with respect to claims 12-22. Therefore, the patent office erred in rejecting claims 12-22 over Aoki in view of Nunogami, Tanaka *et al.*, Aizaki and in further view of LaRue *et al.* under 35 U.S.C. § 103(a).

Summary

For the reasons stated above, Appellant respectfully requests withdrawal of the rejections, reconsideration, and allowance of claims 1-25.

Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Appeal Brief, P.O. Box 1450, Alexandria, VA 22313-1450, on this 12th day of April, 2004.

DANNY PADYS _____

Name Signature

Appendix

1. An logic unit comprising:

a first logic unit connected to a first supply voltage;

a second logic unit connected to a second supply voltage; and

a voltage-level converter connecting the first logic unit to the second logic unit, the voltage-level converter including at least one transistor having a threshold voltage greater than or about equal to the difference between the second supply voltage and the first supply voltage and the at least one transistor connected to the second supply voltage.

2. The logic unit of claim 1, wherein the first logic unit comprises a memory unit.

3. The logic unit of claim 2, wherein the second logic unit comprises an arithmetic unit.

4. The logic unit of claim 3, wherein the one transistor comprises an insulated-gate field-effect transistor.

5. The logic unit of claim 4, wherein the insulated-gate field-effect transistor comprises a p-type insulated-gate field-effect transistor.

6. The logic unit of claim 1, wherein the voltage-level converter comprises an inverter.

7. The logic unit of claim 6, wherein the inverter comprises an n-type insulated-gate field-effect transistor connected in series with the at least one transistor.

8. The logic unit of claim 6, wherein the second logic unit comprises a clock distribution circuit.

9. The logic unit of claim 6, where the voltage-level converter comprises a first inverter coupled in series to a second inverter.

10. The logic unit of claim 9, wherein the first inverter includes the at least one transistor.

11. A logic unit comprising:

a first logic unit connected to a first supply voltage;

a second logic unit connected to a second supply voltage; and

a logic circuit connecting the first logic unit to the second logic unit, the logic circuit including at least one transistor having a threshold voltage greater than or about equal to the difference between the second supply voltage and the first supply voltage and the at least one transistor connected to the second supply voltage .

12. The logic unit of claim 11, wherein the logic circuit comprises an AND circuit.

13. The logic unit of claim 11, wherein the logic circuit comprises a NAND circuit.

14. The logic unit of claim 11, wherein the logic circuit comprises an OR circuit.

15. The logic unit of claim 11, wherein the logic circuit comprises a NOR circuit.

16. The logic unit of claim 11, wherein the logic circuit comprises an XOR circuit.

17. The logic unit of claim 11, wherein the second logic unit comprises a clock distribution circuit.

18. The logic unit of claim 17, wherein the logic circuit comprises a NAND circuit.

19. The logic unit of claim 17, wherein the logic circuit comprises a NOR circuit.

20. The logic unit of claim 11, wherein the second logic unit comprises an arithmetic unit.

21. The logic unit of claim 20, wherein the logic circuit comprises an OR circuit.

22. The logic unit of claim 20, wherein the logic circuit comprises an XOR circuit.

23. A method comprising:

transmitting a logic signal from a logic unit having an output voltage swing between a first voltage level and a second voltage level, the first voltage being greater than the second voltage level;

receiving the logic signal at a logic circuit having a pull-up transistor and an output voltage swing between a third voltage level and a fourth voltage level, the third voltage being greater than the fourth voltage level; and

turning off the pull-up transistor when the logic signal has a value slightly greater than the difference between the third voltage level and the first voltage level, the third voltage level being greater than the first voltage level.

24. The method of claim 23, further comprising:

generating an output logic signal at the logic circuit, the output logic signal having a voltage swing between the third voltage level and the fourth voltage level; and

receiving the output logic signal at an inverter having an output voltage swing between the third voltage level and the fourth voltage level.

25. The method of claim 23, further comprising:

generating an output logic signal at the logic circuit, the output logic signal having a voltage swing between the third voltage level and the fourth voltage level; and

receiving the output logic signal at a logic circuit having an output voltage swing between the third voltage level and the fourth voltage level.